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NANOENGINEERED THERMAL MATERIALS BASED  
ON CARBON NANOTUBE ARRAY COMPOSITES

Cross Reference To Related Applications:

5           This application claims the benefit of U. S. Patent Application (ARC-15042-1), which is incorporated by reference herein.

Origin of the Invention:

          The invention described herein was made by employees of the United States Government and may be manufactured and used by or for the Government for  
10   governmental purposes without the payment of any royalties thereon or therefor.

Technical Field:

          The present invention provides thermal conductors for small components and devices, using carbon nanotube arrays.

Background of the Invention:

15           State-of-the-art integrated circuits (ICs) for microprocessors routinely dissipate power densities on the order of 50 Watts/cm<sup>2</sup>. This large power is due to the localized heating of ICs operating at high frequencies, and must be managed for future high-frequency microelectronic applications. As the size of components and devices for ICs and other appliances becomes smaller, it becomes more  
20   difficult to provide heat dissipation and transport for such components and devices. A thermal conductor for a macro size thermal conductor is generally inadequate for use with a micro size component or device, in part due to scaling problems.

          One consequence of increased component density in, and compactness of, ICs manifests itself in the form of locally high power consumption. An alarming  
25   rise in power density with respect to each advancing technology generation has

been observed in mainstream microprocessor technologies. The need for addressing this problem is imperative for next-generation IC packaging technology. One potential solution is to find new packaging materials that exhibit high thermal conductivity and that can transfer heat from a local hot spot to a larger heat sink.

The cooling of an object by attaching it to a cold reservoir is normally limited by the heat transfer rate across the interface. Except for objects with atomically flat surfaces, practical objects normally have only a very small portion of surface in contact with other solid surfaces. Eutectic bonding materials or thermal conducting pastes/films are normally applied at the interface to increase the contact area. However, the thermal conductivities of these eutectic bonding materials are normally orders of magnitude lower than those of solid materials such as Cu and Si. The interface thus remains the bottleneck for heat dissipation. Metal film can be used to improve the thermal conductivity but is only applicable for high pressure loading.

What is needed is a compliant thermal interface material that efficiently and promptly dissipates or conducts heat from a micro size component or device, preferably down to nanometer scale systems, to a heat sink with a heat transfer rate that is comparable to rates for macro size components and devices. Preferably, the thermal conductor should be reusable and should work with any surface, rough or smooth.

#### Summary of the Invention:

These needs are met by the invention, which uses an embedded carbon nanotube array to provide one or more high performance thermal conductors for applications that require large heat dissipation. This approach also improves the mechanical strength of carbon nanotubes (CNTs) so that the CNT array can remain

stable and can make good contact to the surface of objects that generate large amount of heat, through use of reversible buckling and bending of exposed portions of the CNTs. The extremely high thermal conductivity along a carbon nanotube axis is employed to transfer heat away from hot spots in a component or device. Copper and other high thermal conductivity materials are deposited to fill interstitial regions or gaps in a first part of a CNT array. This composite structure provides mechanical strength to maintain the CNTs in position and also serves as an efficient heat transfer material to improve diffusion of heat flux from an individual CNT to a larger surrounding volume.

The innovation uses vertically oriented CNT arrays to increase the effective contact area (particularly for a rough surface) while providing an extremely large thermal conductivity along a CNT axis and across the interface. The fabrication involves four steps: (1) substantially vertically aligned CNT arrays with a preferred length of from 1 to 50 microns are grown on a solid substrate (serving as a heat sink) that has good thermal conductivity, such as Si wafers and metal blocks/films; (2) a first portion of, or all of, interstitial spaces between adjacent CNTs are filled with highly thermally conductive materials such as Cu, Ag, Au, Pt or doped Si by chemical vapor deposition (CVD), physical vapor deposition (PVD), plasma deposition, ion sputtering, electrochemical deposition, or casting from liquid phase; (3) filler materials are removed from a second portion of the interstitial spaces by mechanical polishing (MP), chemical mechanical polishing (CMP), wet chemical etching, electrochemical etching, or dry plasma etching so that the top portion of the CNT array is exposed, with the bottom part remaining embedded in the filler materials; and (4) the embedded CNT array is applied against an object that is to be cooled. CNTs can reversibly buckle or bend one by one under low loading pressure so that a CNT can make maximum contact with the object to be cooled, even an object with a very rough surface.

Heat can be effectively transferred from the contacting spots along the tube axis to the filler materials as well as the substrates. The filler materials plays two critical roles: (a) improving the mechanical stability, and (b) maximizing the thermal conductivity. Choosing highly thermal conductive materials as the filler matrix maximizes the heat transfer from the contact spots to the substrate (i.e. the heat sink or cooling reservoir). An embedded CNT array can be reused without damage or compromise of its heat transport characteristics, in contrast to an approach that relies upon eutectic bonding.

The invention improves the mechanical stability of a CNT array by anchoring the lower portion of the array in a solid matrix so that the array retains the integrity when pressed against the heated object during mounting processes. The reversible buckling and bending properties of a CNT array ensures a maximum physical contact under a low loading pressure with the object surface, whether the surface is atomically flat or very rough.

For a discrete multiwall carbon nanotube (MWCNT), the thermal conductivity is expected to surpass  $3000 \text{ Watts(meter)}^{-1}\text{K}^{-1}$  along the tube axis, according to P. Kim et al, Phys. Rev. Lett., vol. 87 (2001) 215502-1. Through the use of DC-biased, plasma-enhanced chemical vapor deposition (PECVD), as demonstrated by B.A. Cruden et al, Jour. Appl. Phys., vol. 94 (2003) 4070, one can fabricate vertically aligned MWCNT arrays (sometimes referred to as carbon nanofiber arrays) on silicon wafers of thickness  $\sim 500 \mu\text{m}$  and demonstrate their possible application as a heat-sink device, conducting large amounts of heat away from a localized area, such as in critical “hot spots” in ICs.

This innovation is an outgrowth of an earlier NASA patent application (NASA Ref. No. ARC-15042-1) which uses a CNT array as an electrical interconnect material embedded in an  $\text{SiO}_2$  matrix. Here, a highly thermal

conductive material, such as Cu, Ag, and/or Si, replaces SiO<sub>2</sub>, used to control electrical conduction in the earlier innovation.

Brief Description of the Drawings:

Figure 1 illustrates a CNT array thermal conduction system constructed according to the invention.

Figure 2 schematically illustrates use of the invention.

Figures 3A and 3C illustrates apparatus used for thermal resistance measurements.

Figure 3B illustrates a packaging architecture used in the prior art.

Figures 4A and 4B are scanning electron microscope (SEM) cross sectional and top-down microphotographs, respectively, of an as-grown multiwall carbon nanotube array.

Figures 5A and 5B are SEM cross sectional and top-down photomicrographs, respectively, of a CNT-Cu composite film.

Figures 6A and 6B are graphical views of thermal resistance versus electrical power measurements for a first control sample and Microfaze (Figure 6A) and for a CNT-only film and for two different CNT-Cu films (Figure 6B).

Figures 7A and 7B are SEM photomicrographs of a CNT-Cu film, taken before and after compressive thermal resistance measurements, respectively.

Description of Best Modes of the Invention:

Figure 1 illustrates a procedure for practicing an embodiment of the invention. In step 11, an array of substantially vertically oriented CNTs is grown on a selected surface of a substrate that has good thermal conductivity. The substrate may be a metal-doped silicide, a diamond film, or a metallic substance having a maximum electrical or thermal conductivity. Whether the array is patterned or not, it is preferable to provide a thin CNT catalyst layer (e.g., Ni, Fe, Co, Pd or Al or a combination thereof) having a layer thickness of 2-50 nanometers

(nm), or more if desired. When the CNT is grown in an electrical field oriented substantially perpendicular to the selected substrate surface, the CNTs can be grown in greater lengths (1-50  $\mu\text{m}$  or more) in a direction substantially parallel to the electrical field direction.

5           In step 12, interstitial spaces between adjacent CNTs are partly or fully filled with a selected filler material that is preferably a good thermal conductor (e.g., Cu, Ag, Au or metal-doped silicon), in order to augment the transport of heat, using chemical vapor deposition (CVD), physical vapor deposition (PVD), plasma deposition, ion sputtering, electrochemical deposition, or casting from liquid phase.  
10       Depending upon the density of CNTs in the array and the filler material, the thermal conductivity of the system is estimated to be in a range of 100-3000 Watts/(meter)-K, which is comparable to the thermal conductivity of oriented graphite.

          In step 13, a top portion of the filler material is removed by mechanical  
15       polishing (MP), chemical mechanical polishing (CMP), wet chemical etching, electrochemical etching, dry plasma etching, or a combination thereof so that the top portion of the CNT array is exposed.

          In step 14 (optional), the thermal conduction system provided by the steps 11, 12 and 13 is pressed or otherwise applied to a surface (atomically smooth,  
20       rough or somewhere in between) of an object from which heat is to be removed so that the exposed portions of the CNTs will bend or buckle.

          Figure 2 schematically illustrates use of the system produced by the procedure of Figure 1 to remove heat from an object 25. An array of CNTs 23-i ( $i = 1, \dots, I$  ( $I = 8$  in Figure 2)) is grown or otherwise provided on a selected surface  
25       of a substrate 21 having an optional catalyst layer 22. A layer of filler material 24, having a depth that allows exposure of an upper portion of each CNT 23-i, is provided, for mechanical strengthening of the CNTs and for improved diffusion of

heat that initially travels only along the CNTs (from the object 25). The CNTs 23-i are pressed against a surface of an object 25, from which heat is to be removed, so that many or all of the CNTs make contact with the (rough) object surface and either bend (23-1, 23-3 and 23-7) or buckle (23-4, 23-6 and 24-8) in order to improve heat transport from the object.

A measurement apparatus, illustrated in Figure 3A, including two copper blocks, 31 and 32, four resistive cartridge heaters (not shown) embedded in the upper block, and a cooling bath 33, is used to measure the thermal resistance of a given material. The upper copper block 31 is preferably surrounded by insulation (not shown) to minimize heat loss to the ambient, with the exception of the one square inch section designed to contact the material 34 to be measured. The clamping pressure on the sample is controlled by pneumatically manipulating the upper block. Heat is delivered to the system by applying a constant power to the cartridge heaters. The steady state temperature difference ( $\Delta T = T_B - T_C$ ) between the two blocks, 31 and 32, with the intervening sample 34, was measured. From these data, the thermal resistance  $R$  of the sample is calculated, as in Eq. (1), where  $Q$  is the total power (in Watts),  $A$  is the sample cross-sectional area,  $C_L$  is the constant heat transfer coefficient and  $T_B$ ,  $T_C$ , and  $T_{amb}$  represent the temperature of the upper block 31, the chilled lower block 32 ( $T_C = 20^\circ\text{C}$ ), and the ambient environment, respectively. The heat transfer coefficient  $C_L$  is used to estimate the heat loss to the ambient environment in this measurement configuration and is determined by placing a thick insulator between the two blocks and measuring the steady state  $\Delta T$  at a variety of applied powers. This analysis yields a constant heat transfer coefficient of  $C_L = 0.0939$  Watts/K, which is factored into the final determination of the measured thermal resistance  $R$ . This coefficient  $C_L$  represents the heat power lost (in Watts) per degree Kelvin to the ambient environment.

$$R = \frac{A(T_B - T_C)}{Q - C_L(T_B - T_{amb})} \quad (1)$$

The dominant thermal resistance mechanism in this measurement configuration is that of the contact interfaces between the sample 34 and the copper blocks, 31 and 32. To minimize this contact resistance, two steps were taken: (1) polishing both copper blocks, 31 and 32, to reduce the effect of surface roughness and (2) making use of a high thermally conductive, conformal material, Microfaze A6 (available from AOS Thermal Compounds, LLC, New Jersey) to reduce contact resistance on the backside of a silicon wafer, the substrate on which the investigated films were fabricated.

## Sample Preparation

Carbon nanotubes were synthesized using the procedure and reactor conditions reported by B.A. Cruden et al, op cit. The resulting as-grown tubes are shown in cross section and top views in Figures 4A and 4B, respectively. Using scanning electron microscope (SEM) data, we estimate the length of the MWCNTs to be about 7.5  $\mu\text{m}$ , with a possible range of 1-50  $\mu\text{m}$ .

Following nanotube synthesis, a high thermal conductivity metal-like substance (e.g., Cu, Ag, Au, Pt or Pd) between individual MWCNTs (also referred to as nanotube trenches) was deposited through electrodeposition, using a three-electrode setup with a one  $\text{cm}^2$  MWCNT array as the working electrode, a Saturated Calomel Electrode (SCE) as the reference electrode, and a one square inch platinum foil as the counter electrode (CE), set in parallel with the MWCNT sample. Both the Cu substrate and the MWCNTs serve as electrodes during the electrodeposition.

Various additives are optionally added to the solution to achieve optimum gap filling into the high-aspect-ratio, forest-like MWCNT arrays. The recipe of the electrolyte solution used in this study is based on the methodology reported for



deep-trench filling of Cu interconnects for damascene processes, as reported by K. Kondo et al, Jour. Electroanalytical Chem., vol. 559(2003) 137. We begin with a stock solution comprised of copper sulfate ( $\text{CuSO}_4 \cdot 5\text{H}_2\text{O}$ ), sulfuric acid ( $\text{H}_2\text{SO}_4$ ), and sodium chloride ( $\text{NaCl}$ ). Polyethylene glycol (PEG) is added to inhibit copper deposition at the tips of the nanotubes when in the presence of  $\text{Cl}^-$  ions. Janus Green B (JGB) is also added for its deposition inhibiting properties. Bis(3-sulfopropyl) disulfide (SPS) is included to increase local current density at the bottom of the nanotube trenches, thus enhancing the superfilling of high-aspect ratio trenches. The final solution, including concentrations used in the bath, is shown in Table I. Typically, the Cu was deposited at  $-0.20$  to  $-0.30$  V (vs. SCE) at a deposition rate of about 430 nm/min. The resulting CNT-Cu composite material is shown in Figures 5A and 5B.

Figure 3C illustrates typical packaging architecture, as discussed by R. Viswanath et al, Intel Tech. Jour Q3 (2000), including a heat sink (fins and heat spreader) 41 are contiguous to a thin interface (phase change film, grease, etc.) 42, which is contiguous to a thin silicon layer 43. A heat delivery array 45 contacts the silicon array back surface 43 through a conductive gel or epoxy 44. This system requires use of greases, phase change films, thermally conductive gels and/or special epoxies and is quite complex.

**Table I.** Electrochemical bath composition for copper deposition

Bath Chemical/Additive (concentration unit)	Concentration
$\text{CuSO}_4 \cdot 5\text{H}_2\text{O}$ (mol/L)	0.6
$\text{H}_2\text{SO}_4$ (mol/L)	1.85
$\text{NaCl}$ (ppm)	100
PEG, molar mass: 8000 (ppm)	400
JGB (ppm)	10
SPS (ppm)	10

## Results and Discussion

To summarize the structure used, Figure 3B illustrates the equivalent thermal resistance model for the CNT-Cu composite sample. The resistance of the CNT-Cu composite can be obtained by de-embedding the thermal resistance contribution of the copper block ( $R_{\text{Cu-block}}$ ), silicon wafer ( $R_{\text{Si}}$ ), and the Microfaze material ( $R_{\mu\text{Faze}}$ ). The thermal resistance of the copper block,  $R_{\text{Cu-block}}$ , must be taken into account due to the placement of the thermocouple (approximately one inch from the copper block surface). From bulk calculations,  $R_{\text{Cu-block}}$  for this configuration can be estimated as  $0.95 \text{ cm}^2\text{K/Watt}$ . To summarize, one can determine the resistance of the CNT/Cu composite film by Eq. (2).

$$R_{\text{CNT/Cu}} = R_{\text{total}} - R_{\text{Cu-block}} - R_{\text{Si}} - R_{\mu\text{Faze}} . \quad (2)$$

$R_{\mu\text{Faze}}$  is determined using two control measurements. The first measurement involves measuring the thermal resistance of a piece of silicon with Microfaze on the backside of the wafer, resulting in  $R_{\text{control}} = R_{\text{Cu-block}} + R_{\text{block-Si}} + R_{\mu\text{Faze}}$ , where  $R_{\text{block-Si}}$  is the interface resistance between the copper block and silicon wafer. The second resistance measurement involves a piece of double-sided polished silicon, resulting in  $R_{\text{control},2} = 2R_{\text{block-Si}} + R_{\text{Si}}$ . Assuming that both Si-Cu interfaces in the second control measurement are similar, one can divide this value in half and use the simple relation in Eq. (3).

$$R_{\mu\text{Faze}} = R_{\text{control},1} - (R_{\text{control},2} - R_{\text{Si}})/2 - R_{\text{Cu-block}} . \quad (3)$$

The intrinsic silicon contribution ( $R_{\text{Si}}$ ) to the thermal resistance in Eqs. (2) and (3) can be neglected. For the  $500 \text{ }\mu\text{m}$  thick silicon wafer used in this study, the intrinsic silicon thermal resistance can be calculated as  $0.034 \text{ cm}^2\text{K/Watt}$ , which is two orders of magnitude less than the final measured values of the CNT-Cu sample, and is thus negligible. One caveat to this analysis is in regards to the thermal resistance of Microfaze with respect to the amount of power applied to the

upper block. The thermal resistance of the first control sample decreases approximately exponentially with increasing power, corresponding to different temperature gradients, but can be corrected for in the final analysis as will be demonstrated. The double-sided, polished silicon sample shows no power  
5 dependence and exhibits a substantially constant resistance of  $R = 11.10 \text{ cm}^2\text{K/Watt}$ , resulting in  $5.55 \text{ cm}^2\text{K/Watt}$  per silicon interface. Subtracting the silicon resistance, which is constant with respect to applied power, one can also determine  $R_{\mu\text{Faze}}$  at different powers. The power dependence of the Microfaze is illustrated in Figure 6A.

10 Now that the power dependence of the Microfaze material is quantified, one proceeds with the analysis of the CNT/Si/Microfaze and CNT-Cu/Si/Microfaze stacks. From the previous discussion, one expects these samples to exhibit the same power dependence, which indeed is the case and is clearly seen in Figure 6B. Combining the power dependence with the measurements in Figure 6B we  
15 summarize the values of measured thermal resistance in Table II. All measurements were performed at similar clamp pressures, 6.8 psi. Errors contributing to the standard deviation in the measurements can be attributed primarily to two factors: (1) variations in contact area due to varying CNT length distribution (see Figure 4A); and (2) variations in measurement of total power,  $\Delta T$ ,  
20 and ambient temperature loss. However, even at the upper bounds of the measured thermal resistance values for the CNT-Cu composite films, this worst-case scenario represents values that are on the order of the thermal budgets for a variety of commercial microprocessor systems.

**Table II.** Thermal Resistance Measurement Summary

<b>Material</b>	<b>Thermal Resistance (cm<sup>2</sup>K/W) <math>\pm</math> STDEV</b>
CNT film	2.30 $\pm$ 0.33
CNT-Cu composite film (#1)	0.84 $\pm$ 0.22
CNT-Cu composite film (#2)	0.92 $\pm$ 0.13
Bare double-sided silicon	11.10 $\pm$ 0.65

The Cu deposited in the MWCNT array used in this study was not a solid  
 5 film. Instead, the Cu forms a porous film with ~70% Cu and CNTs and ~30%  
 voids. This configuration increases the mechanical strength so that the sample can  
 be repeatedly and reproducibly measured under different clamping pressures. In  
 addition, this configuration provides spaces so that the composite film can be  
 deformed to make maximal contact with the hot surface. However, studies  
 10 conducted on the buckling force of discrete MWCNTs, by H Dai et al, Nature, vol.  
 384 (1996) 147, by H. Dai et al, Appl. Phys. Lett. Vol. 73 (1998) 1508, and by J.  
 Li et al (Surf. And Interf. Analysis, vol. 28 (1999) 8, demonstrate the tremendous  
 amount of force per unit cross sectional area that these structures can withstand.  
 Based on this analysis, we speculate that most nanotubes do not buckle under the  
 15 force applied in this preliminary study, which is roughly two orders of magnitude  
 less than the calculated CNT buckling force. SEM characterization before and  
 after the thermal resistance measurement (Figures 7A and 7B, respectively) shows  
 no effect on the CNT-Cu composite after compressive stress. This approach  
 assumes that most CNTs are bent or buckled to give maximum contact under low  
 20 pressure (no more than 20 psi in IC packaging), which pressure can be achieved by  
 suitable choice of length and diameter of exposed portions of the CNTs

The thermal resistance at the interface can be further reduced by optimizing the invented interface materials and packaging technology. More particularly, the contact area at low loading pressure (less than 20 psi) can be increased by optimizing the length of the exposed CNTs (which results in lower buckling and bending force). The thermal conductivity of Cu filled in interstitial space can be also increased by improving the integrity of the Cu material. With such optimization implemented, the thermal resistance is expected to be reduced below  $0.1 \text{ cm}^2\text{K/Watt}$  which is even better than eutectic binding used today, and can be efficiently used for heat dissipation over  $100 \text{ Watts/cm}^2$  for future IC chips.

These preliminary results demonstrate the fundamental usefulness of CNTs and CNT-Cu composite films as efficient heat conductors. Our analysis confirms that these novel thermal conductivity layers can accomplish effective heat conduction by increasing contact area. In addition, the CNTs provide the added benefits of high mechanical stability and reusability.